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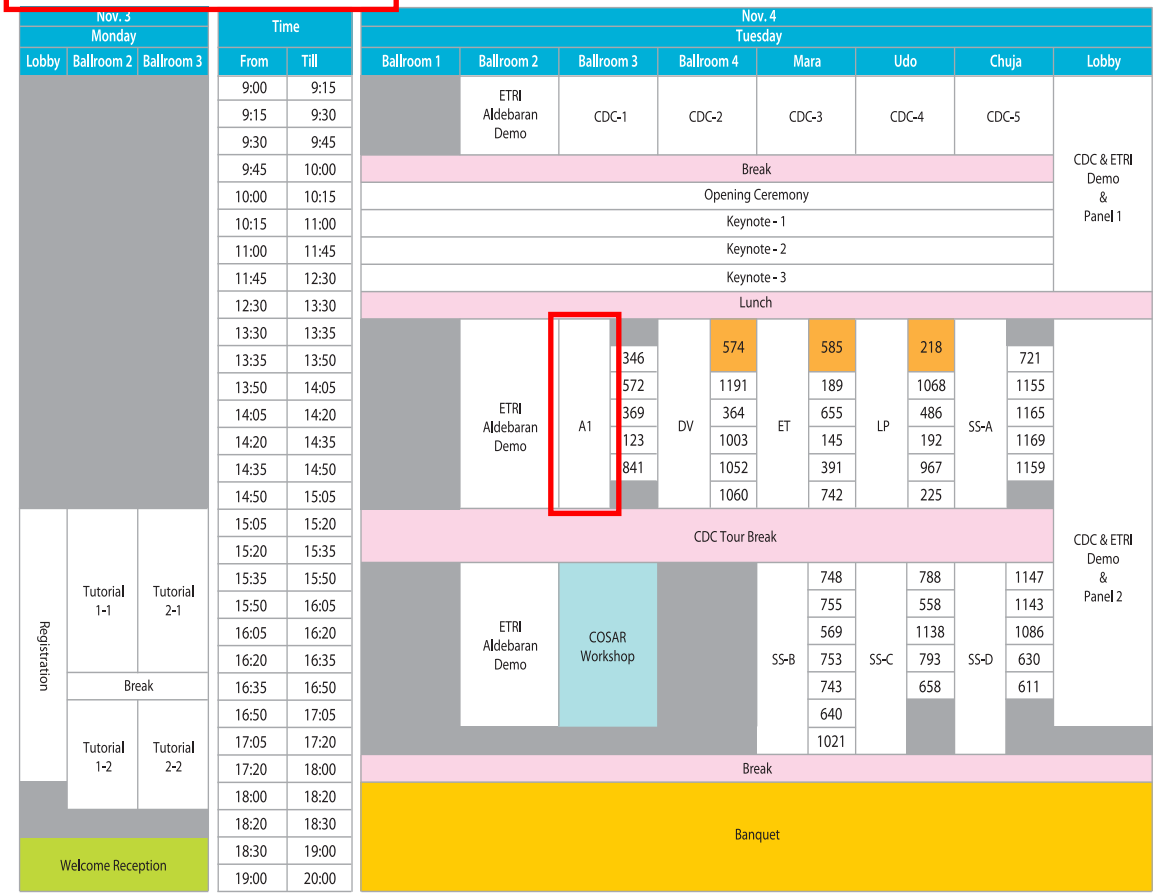
Time Table

Monday ~ Tuesday, November 3~4, 2014



A1 Analog and Mixed-Signal Techniques I

DV Digital Circuits and VLSI Architectures

ET Emerging technology

LP Power Electronics / Energy Harvesting Circuits

SS-A Invited Special Session: Near-Threshold Voltage Circuit Design

SS-B Invited Special Session: Image Signal Processing for Vision/Multimedia SoC

SS-C Invited Special Session: Analog/Digital Circuits for Mobile SoC

SS-D Invited Special Session: Design, Analysis and Tools for Integrated Circuits and Systems (DATICS)

Oral Session

Tuesday, November 4, 2014

A1

Analog and Mixed-Signal Techniques I

13:35~14:50 Ballroom 3

Chair: Hung-Wen Lin *(YuanZe University, Taiwan)*

DV

Digital Circuits and VLSI Architectures

13:30~15:05 Ballroom 4

Chair: Saleh Abdel-hafeez *(Jordan University of Science and Technology, Jordan)*

12.5-Gb/s Monolithically Integrated Optical Receiver With CMOS Avalanche Photodetector

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Abstract

We present a 12.5-Gb/s monolithically integrated optical receiver with CMOS avalanche photodetector (CMOS-APD) realized in 65-nm CMOS technology. The optical detection bandwidth limitation of CMOS-APD due to the carrier transit time is compensated by underdamped TIA. With this optical receiver, 12.5-Gb/s 850-nm optical data are successfully detected with bit-error rate less than 10^{-12} at the incident optical power of −2 dBm. The fabricated optical receiver has the core size of 0.24 × 0.1 mm^2 and its power consumption excluding output buffer is about 13.7 mW with 1.2-V supply voltage.

Keywords—Avalanche photodetectors (APDs); Monolithic integration; Optical interconnects; Optical receiver;

Introduction

Recently, optical interconnect technology is receiving a great amount of research attention as it can overcome the limitation of electrical interconnect bandwidth. 850-nm optical interconnects based on vertical-cavity surface-emitting lasers (VCSELs) and multimode fibers (MMFs) have found many applications for short-reach interconnects such as chip-to-chip, board-to-board and rack-to-rack interconnects [1]. With realization of high-speed photodetectors (PDs) in standard complementary metal-oxide-semiconductor (CMOS) process, monolithically integrated 850-nm Si optical receivers can be realized, which provides cost effectiveness and high-volume manufacturability as well as performance improvement without parasitic pad capacitance and bonding wire inductance.

Several monolithically integrated optical receivers on standard CMOS technology for 10-Gb/s applications have been reported [2-5]. PDs realized in standard CMOS technology do not have the optimal PD strcture and, typically, have very limited bandwidth. To overcome this, CMOS optical receivers including spatially-modulated photodetectors (SM-PDs) [3] or on-chip equalizers [5] have been reported. However, they have low responsivity and require additional power and area.

In this paper, we demonstrate another technique of overcoming the PD bandwidth. We intentionally design underdamped transimpedance amplifier (TIA) which can compensate CMOS-APD bandwidth limitation and result in enhanced overall bandwidth performance. With this design approach, we successfully demonstrate 12.5-Gb/s operation.

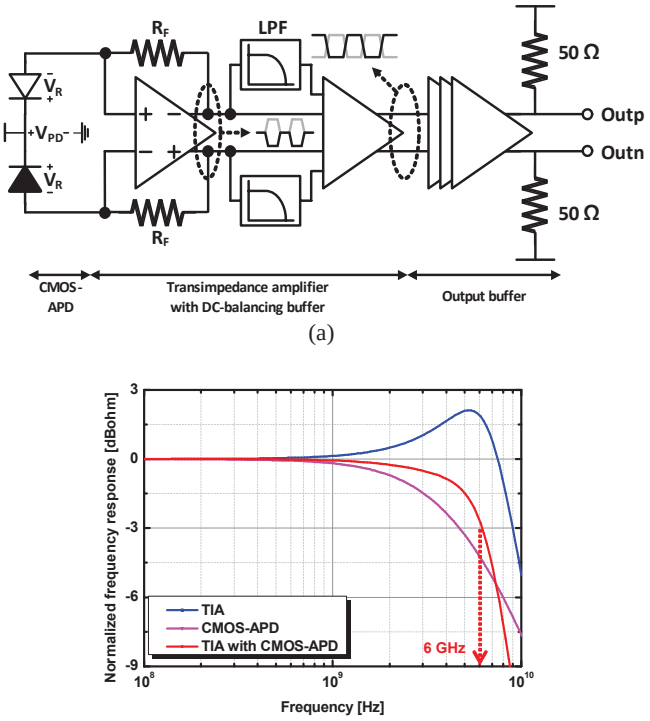

Fig. 1. (a) Block diagram of the proposed optical receiver and (b) simulated frequency responses.

Optical Receiver Circuit

Fig. 1(a) shows a simplified block diagram of our optical receiver. It is composed of a CMOS-APD with a dummy PD, a shunt-feedback TIA with DC-balancing buffer, and output buffer with 50-Ω load. The dummy PD provides symmetric capacitance to the differential TIA input. With CMOS-APD, the photo-detection bandwidth of our CMOS-APD is limited by the transit time of slow diffusive photocurrents. This leads to the bandwidth limit in optical receiver even with a high-speed TIA. To compensate this, we use an underdamped TIA which can be realized by decreasing the core-amplifier bandwidth of shunt-feedback TIA. Fig. 1(b) shows the simulated frequency responses for the transit time response of the PD used in our receiver, electrical response TIA with junction capacitance of used PD, and the final response with the PD and the TIA. As shown in Fig. 1(b), high-frequency peaking of the uderdamped TIA leads to bandwidth

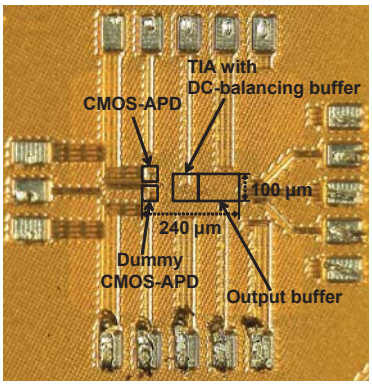

Fig. 2. Microphotograph of the fabricated optical receiver.

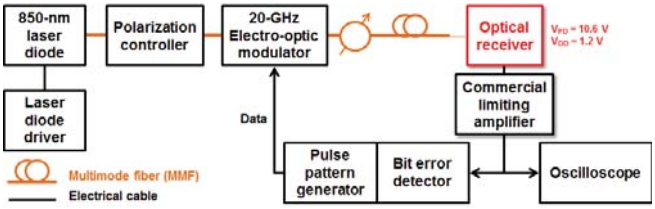

Fig. 3. Measurement setup for data transmission.

enhancement of the total receiver frequency response.

Photo-generated currents from one port of differential TIA generate TIA differential output with a DC offset which can cause decision threshold problem. To eliminate this problem, a DC-balancing buffer is added.

Experiment Result

Fig. 2 shows the micro photograph of the fabricated optical receiver in 65-nm CMOS technology. The core size is 0.24 × 0.1 mm^2, and the power consumption of the electronic circuit excluding output buffer is about 13.7 mW with 1.2-V supply voltage.

Fig. 3 shows the measurement setup for optical data transmission. All experiments are done on-wafer. The 850-nm modulated optical signals are generated by an 850-nm laser diode and a 20-GHz external electro-optic modulator. The modulated optical signals are transmitted through MMF and injected into the optical receiver with lensed fiber. The applied bias voltage of CMOS-APD is experimentally optimized for BER performance at 10.6 V. For bit-error rate (BER) measurement, a 12.5-Gb/s commercial limiting amplifier is used to satisfy the input sensitivity requirement of BER test equipment. Fig. 4 shows the measured BER performance with various incident optical power. The 12.5-Gb/s PRBS7 data detection is successfully achieved and the measured 10^{-12} BER is −2 dBm. The inset in Fig. 4 shows the measured eye diagram for 12.5-Gb/s data transmission with −2-dBm incident optical power.

Conclusion

A 12.5-Gb/s monolithically integrated optical receiver with CMOS-APD is realized in 65-nm CMOS technology. With careful design of TIA so that it can compensate the bandwidth limit of the CMOS-APD, the 3-dB bandwidth is enhanced and

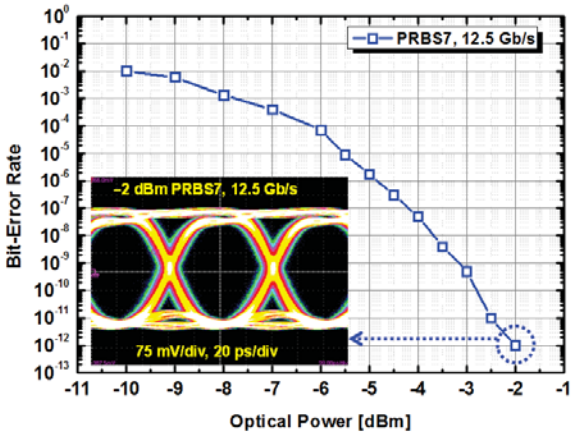

Fig. 4. Measured BER performance and eye diagram of transmitted 12.5-Gb/s data.

12.5-Gb/s optical data are successfully detected.

Acknowledgment

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References

[1] T.-K. Woodward and A. V. Krishnamoorthy, "1-Gb/s integrated optical detectors and receivers in commercial CMOS technologies," *IEEE J. Sel. Top. Quantum Electron.*, vol. 5, no. 2, pp. 146-456, Mar. 1999.

[2] S.-H. Huang, W.-Z. Chen, Y.-W. Chang, and Y.-T Huang, "A 10-Gb/s OEIC with meshed spatially-mudulated photo detector in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1158-1169, May 2011.

[3] M.-J. Lee, J.-S. Youn, K.-Y. Park, and W.-Y. Choi, "A fully-integrated 12.5-Gb/s 850-nm CMOS optical receiver based on a spatially-modulated avalanche photodetector," *Opt. Express*, vol. 22, no. 3, pp. 2511-2518, Feb. 2014.

[4] D. Lee, J. Han, G. Han, and S. M. Park, "An 8.5-Gb/s fully integrated cmos optoelectronic receiver using slope-detection adaptive equalizer," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2861-2873, Dec. 2010.

[5] J.-S. Youn, M.-J. Lee, K.-Y. Park, and W.-Y. Choi, "10-Gb/s 850-nm CMOS OEIC receiver with a silicon avalanche photodetector," *IEEE J. Quantum Electron.*, vol. 48, no. 2, pp. 229-236, Feb. 2012.